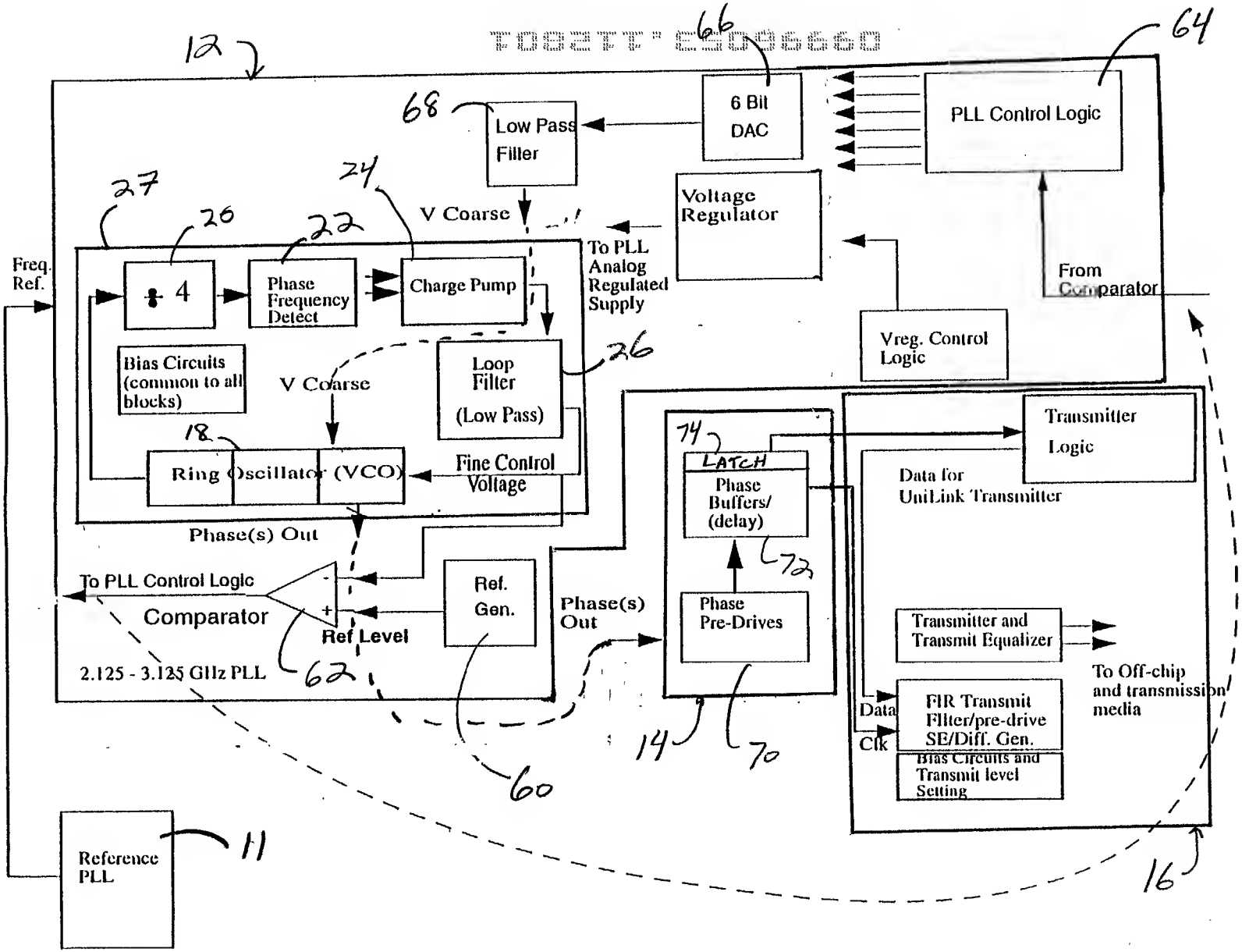

12
66
64
68
Low Pass Filter
6 Bit DAC
PLL Control Logic
27
24
26
22
V Coarse
Voltage Regulator
To PLL Analog Regulated Supply
From Comparator
Freq. Ref.
÷ 4
Phase Frequency Detect
Charge Pump
Bias Circuits (common to all blocks)
V Coarse
Loop Filter (Low Pass)
Vreg. Control Logic
26
18
Ring Oscillator (VCO)
Fine Control Voltage
Transmitter Logic
74
LATCH
Phase Buffers/ (delay)
Data for UniLink Transmitter
Phase(s) Out
72
To PLL Control Logic
Comparator
Ref Level
Ref. Gen.
Phase(s) Out
Phase Pre-Drives
Transmitter and Transmit Equalizer
To Off-chip and transmission media
2.125 - 3.125 GHz PLL
62
Data
Clk
FIR Transmit Filter/pre-drive SE/Diff. Gen.
Bias Circuits and Transmit level Setting
14
70
60
16
Reference PLL
11
10

FIGURE 1.

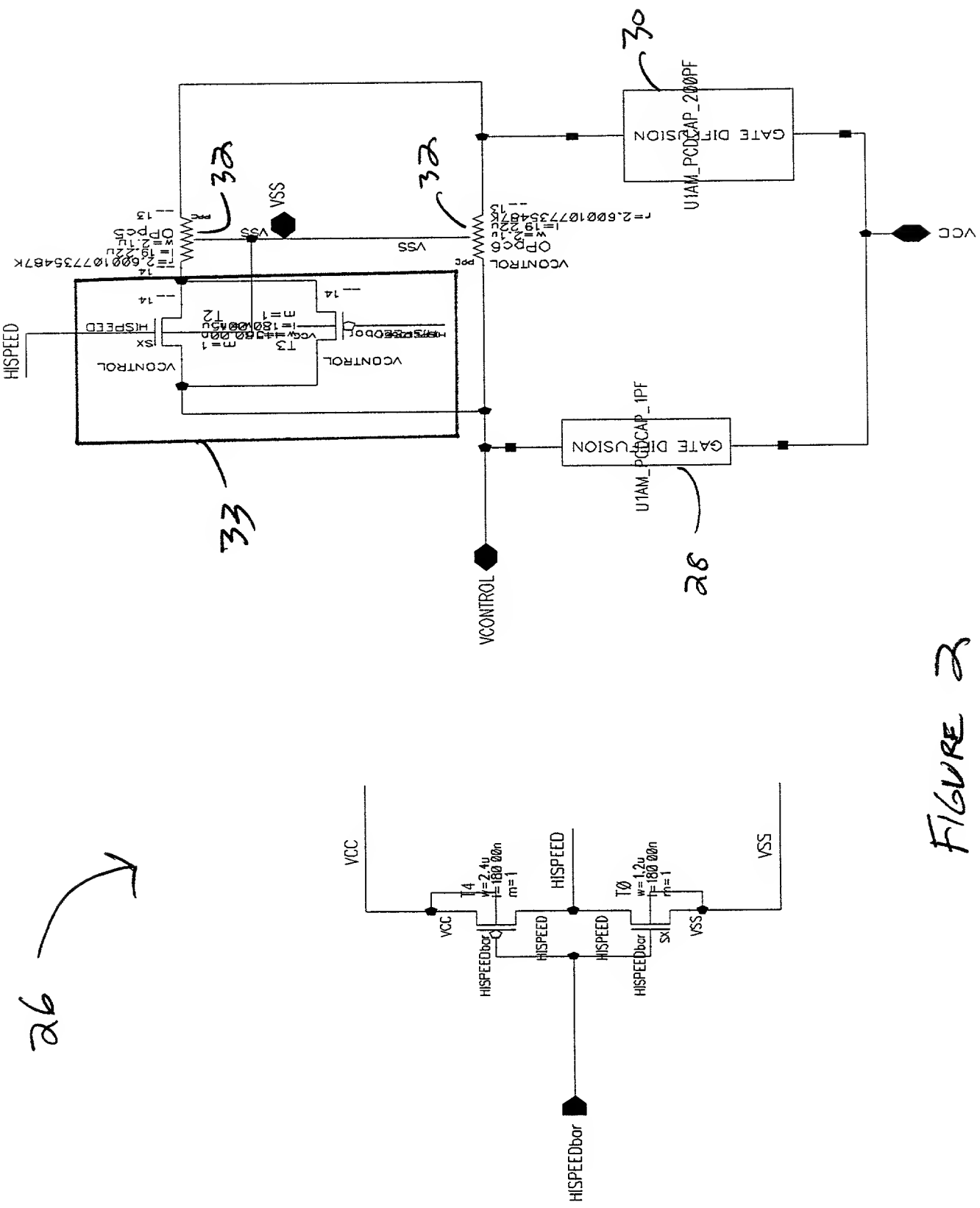

26
VCC
VSS
HISPEEDbar
HISPEED
T4
T0
VCONTROL
GATE DIFFUSION
U1AM_PCCCAP_200PF
U1AM_PCCCAP_1PF
30
32
33
28

FIGURE 2

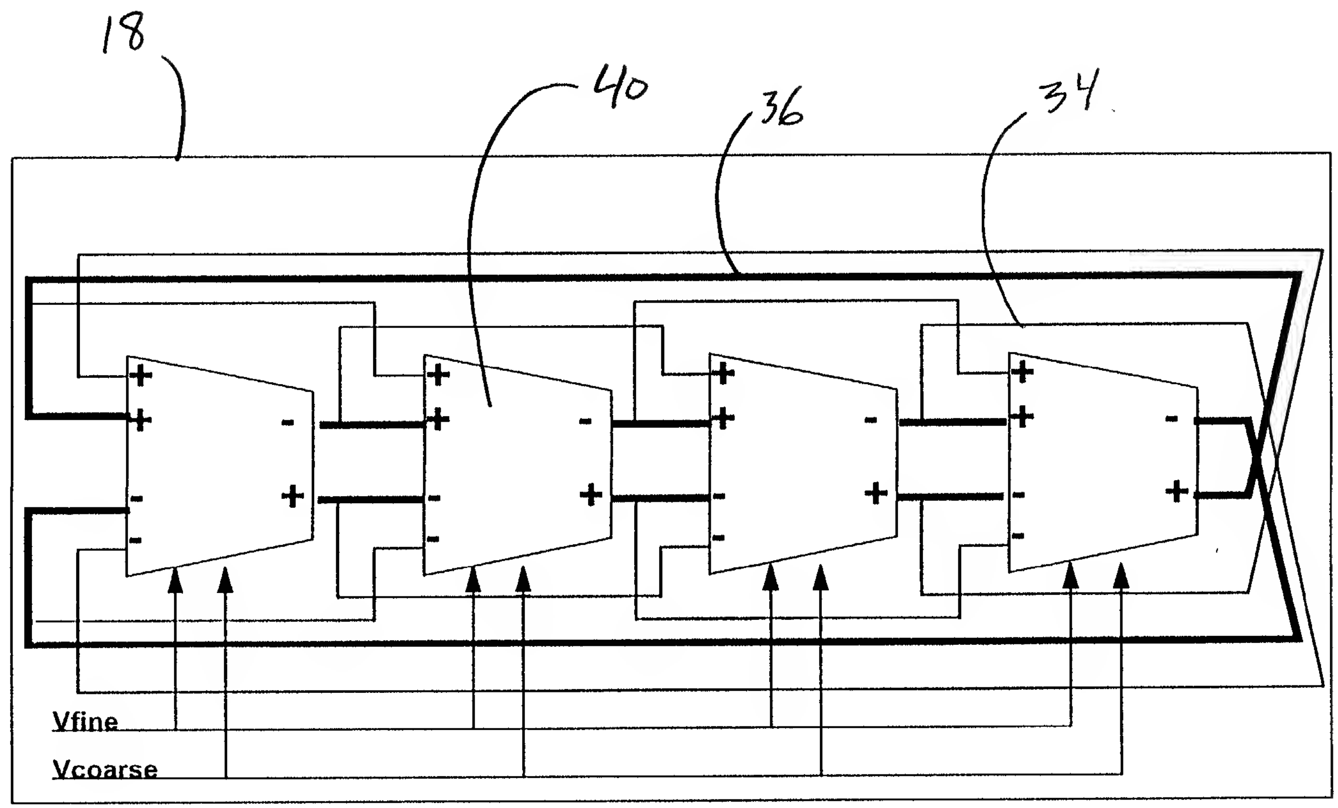


FIGURE 3

(FIGURE 17, p 48)

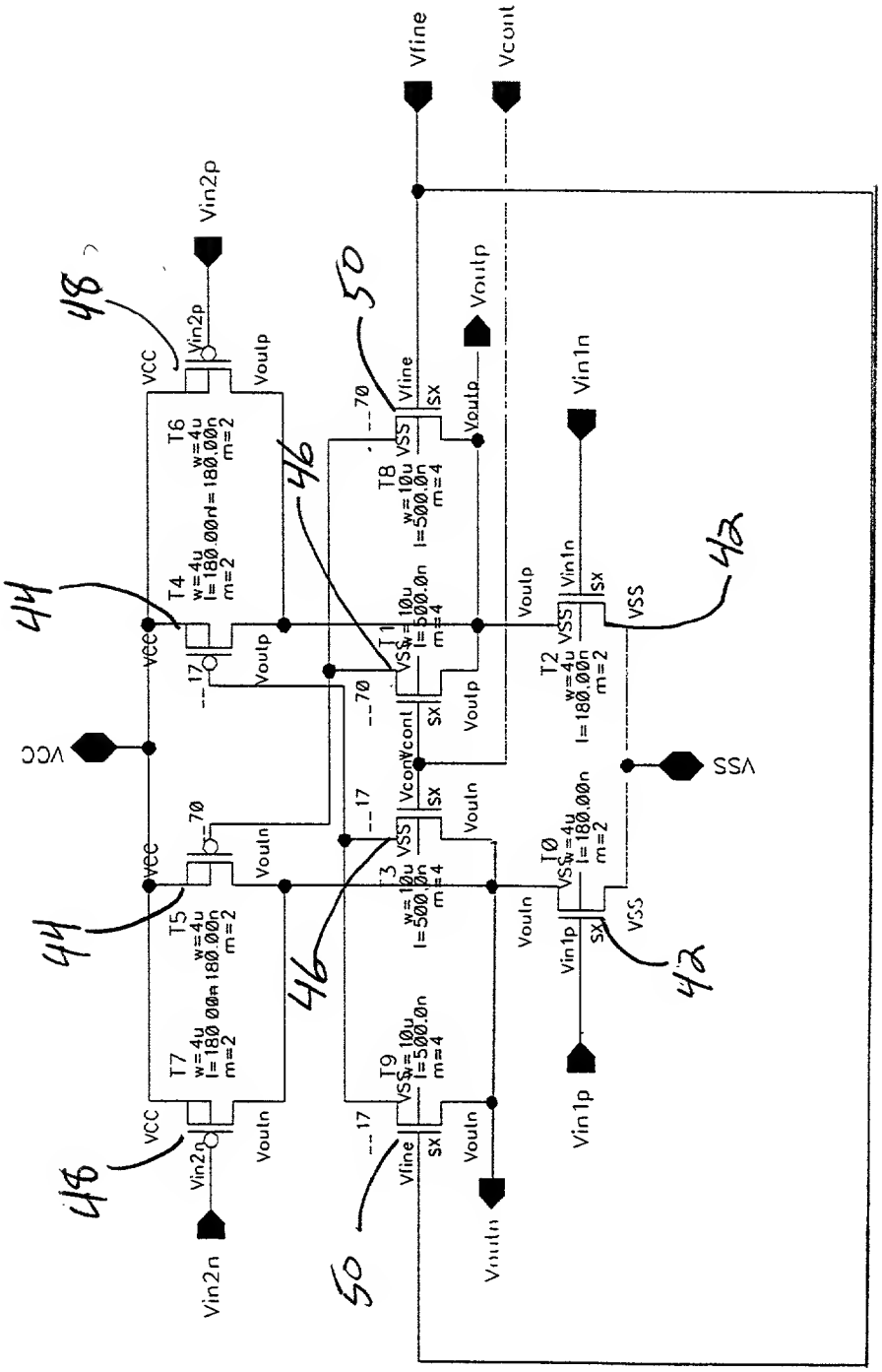


FIGURE 4

(Figure 4, Page 4/26)

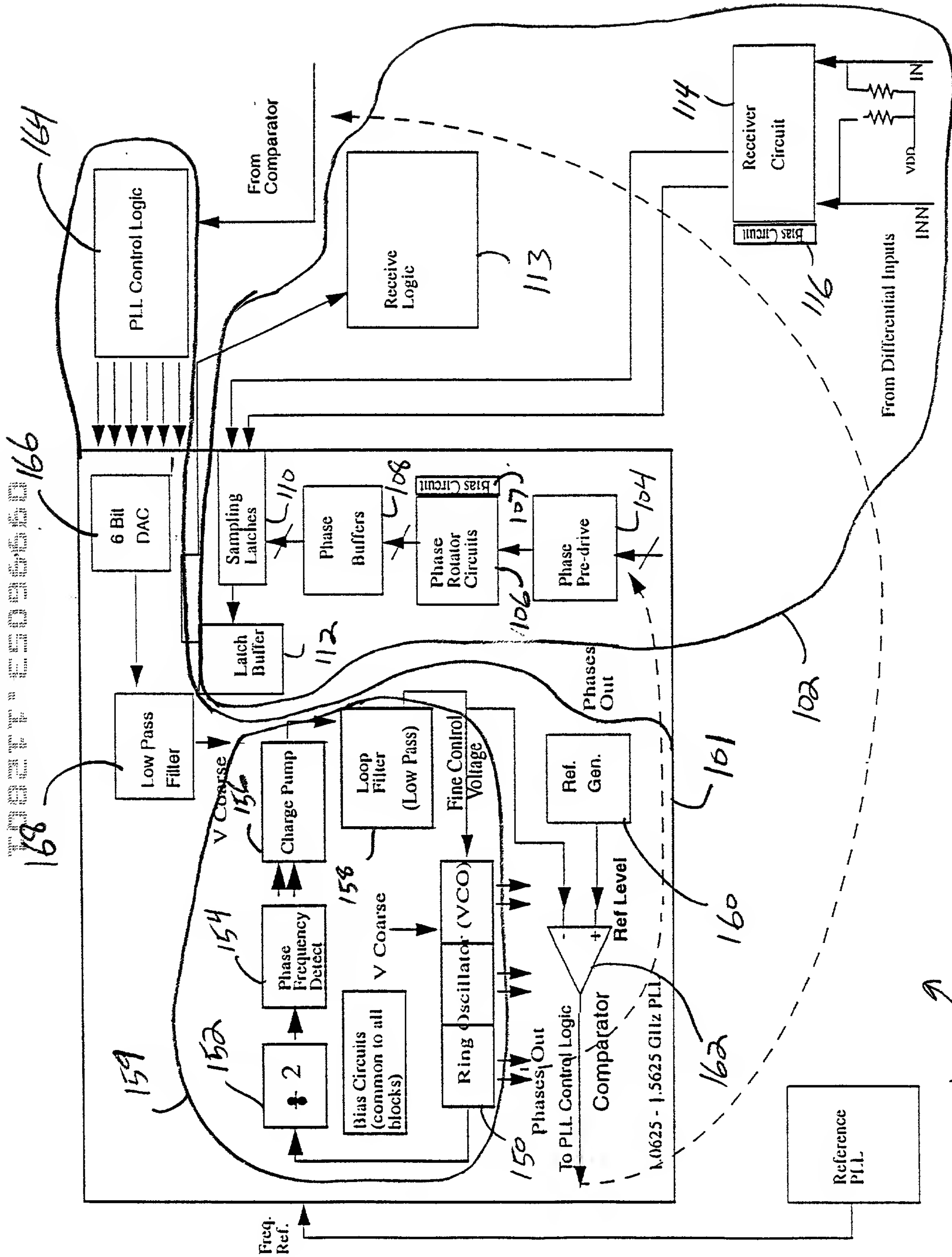

PLL Control Logic
From Comparator
Receive Logic
Receiver Circuit
Bias Circuit
VDD
IN
INN
From Differential Inputs
6 Bit DAC
Sampling Latches
Phase Buffers
Bias Circuit
Phase Rotator Circuits
Phase Pre-drive
Latch Buffer
Low Pass Filter
Phases Out
V Coarse
Charge Pump
Loop Filter (Low Pass)
Fine Control Voltage
Ref. Gen.
Phase Frequency Detect
V Coarse
Ring Oscillator (VCO)
÷ 2
Bias Circuits (common to all blocks)
Phases Out
To PLL Control Logic
Comparator
Ref Level
1.0625 - 1.5625 GHz PLL
Reference PLL
Freq. Ref.
164
166
168
113
114
116
110
108
107
104
106
112
102
101
160
162
150
152
154
156
158
159
100

FIGURE 5

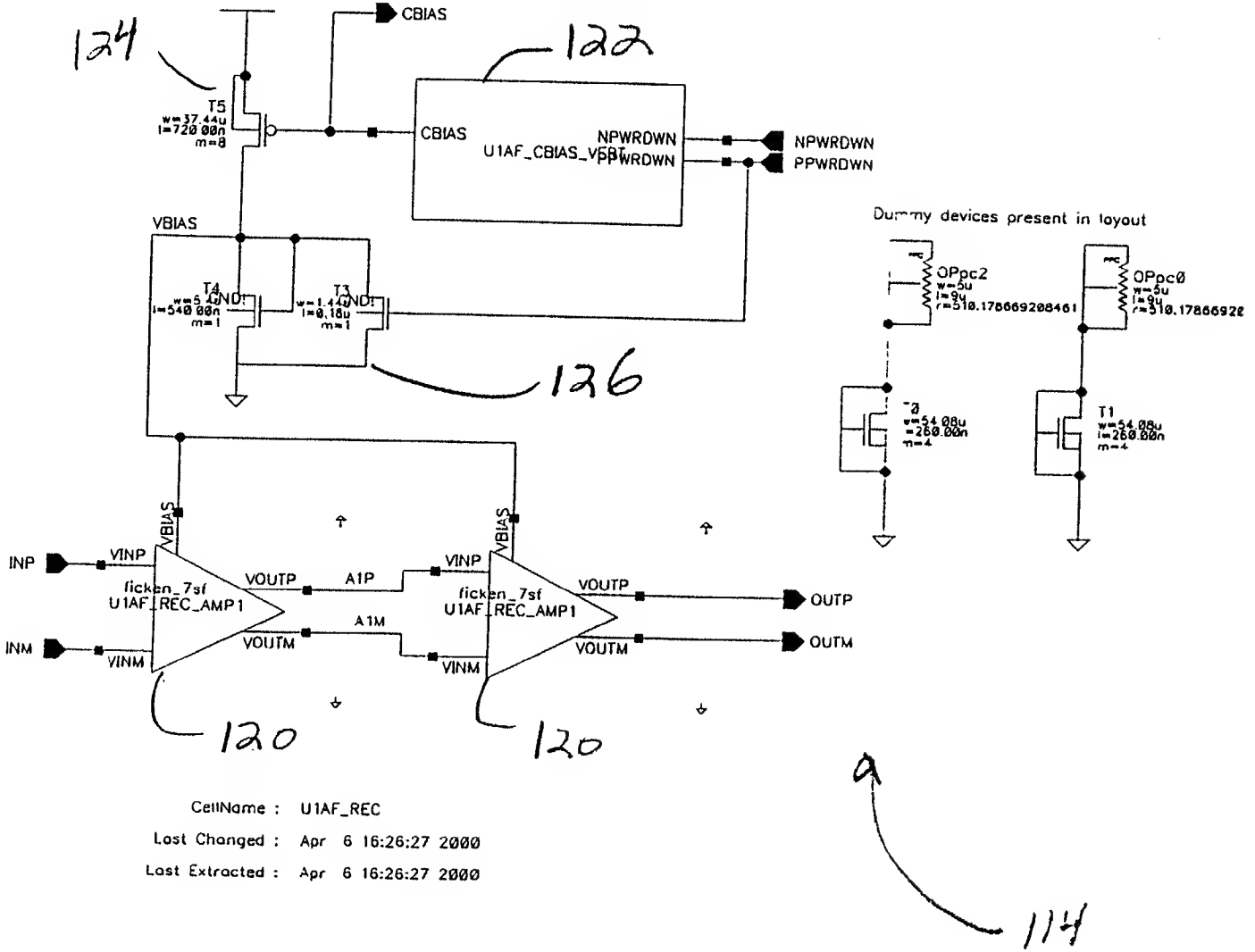


FIGURE 6

FIGURE 55, page 102

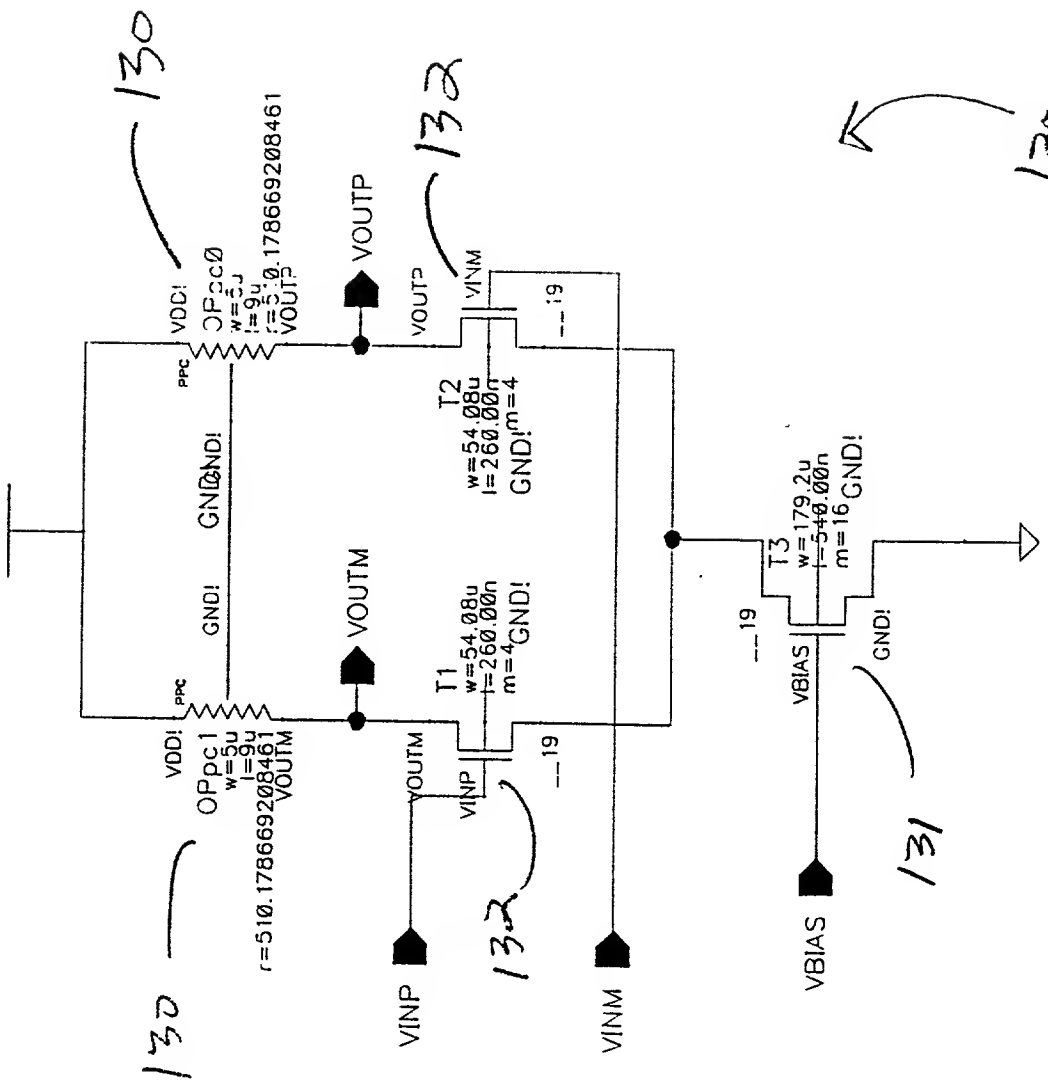


FIGURE 7

(FIGURE 56, p. 103)

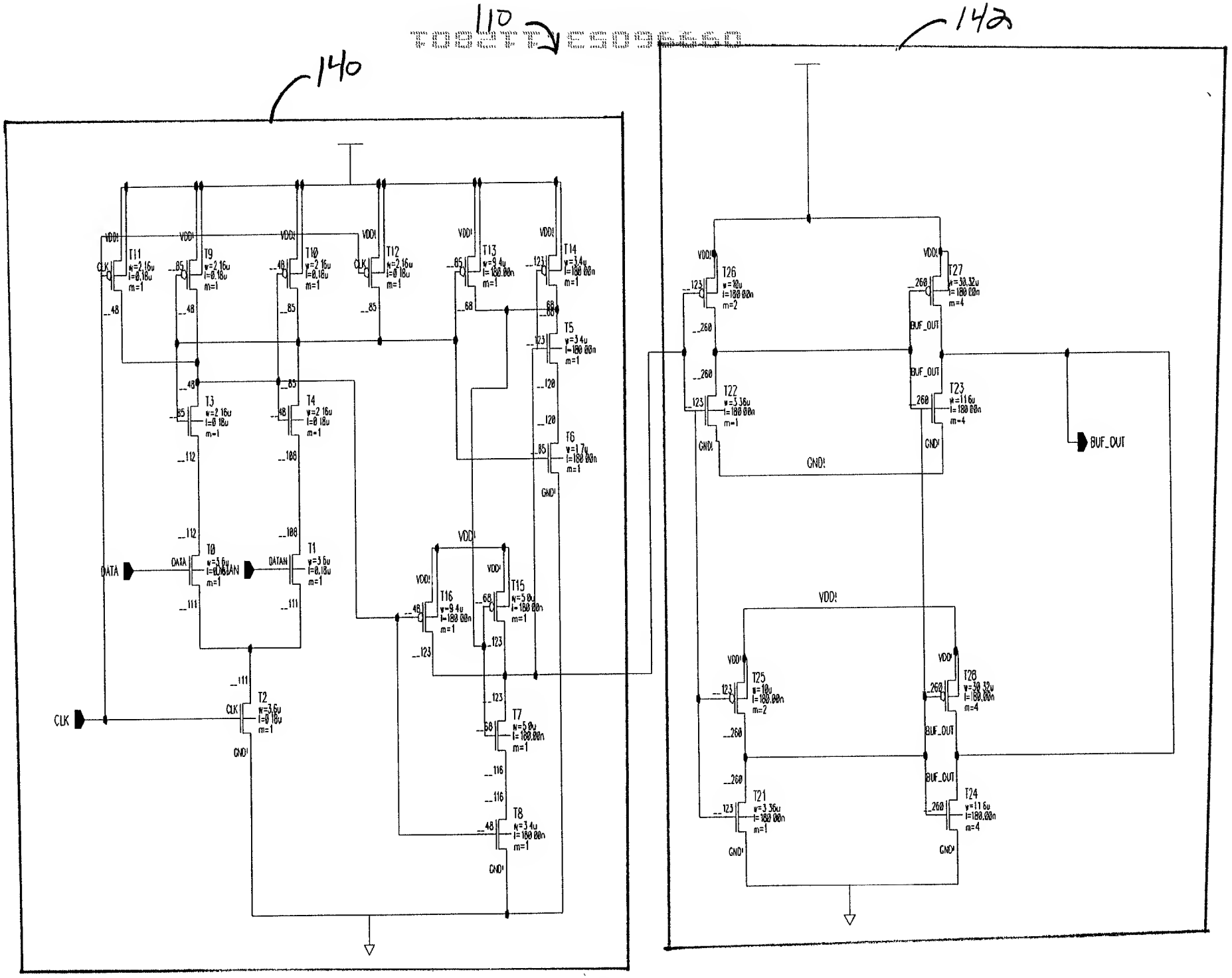

110
140
142
VDD!
GND!
CLK
DATA
DATAN
BUF_OUT
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T21
T22
T23
T24
T25
T26
T27
T28

FIGURE 8

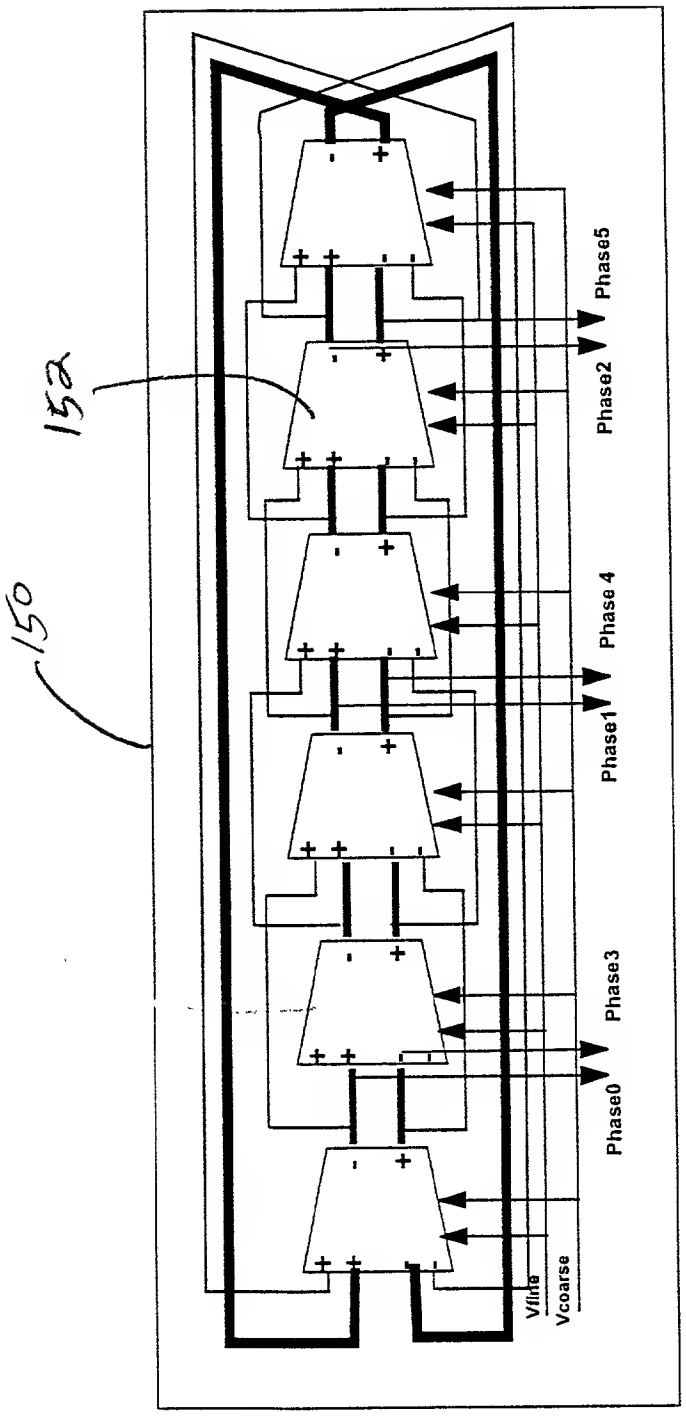

152
150
Phase5
Phase2
Phase 4
Phase1
Phase3
Phase0
Vfine
Vcoarse

FIGURE 9

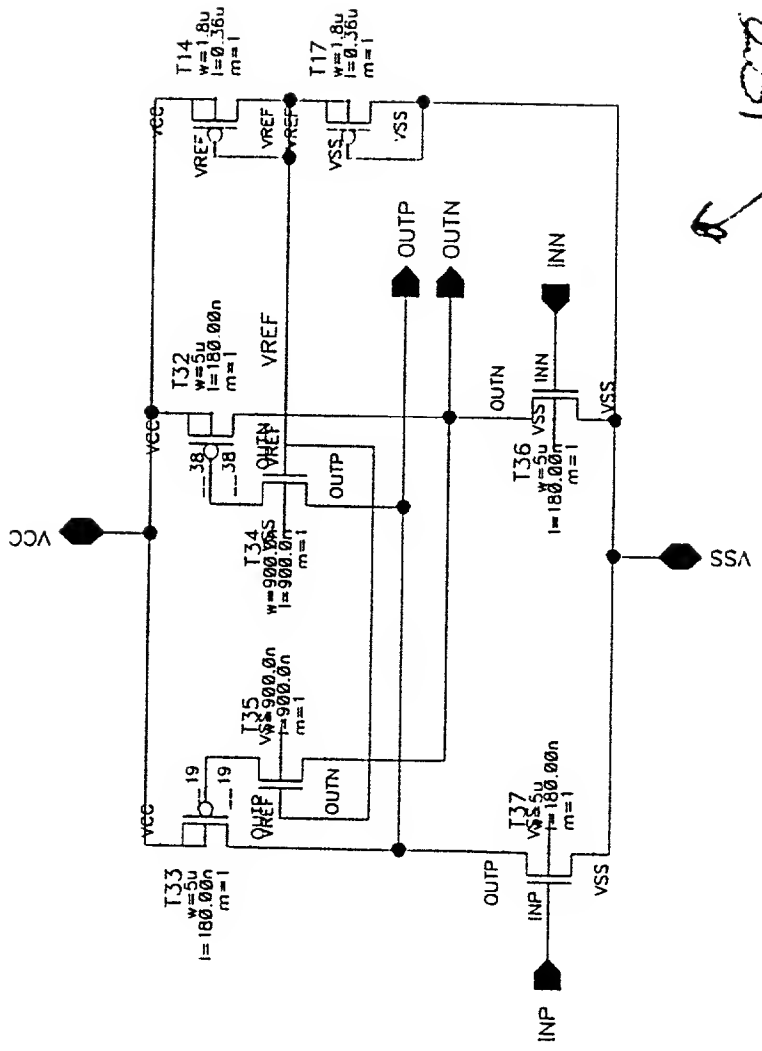


FIGURE 1D

(FIGURE 3D, page 70)

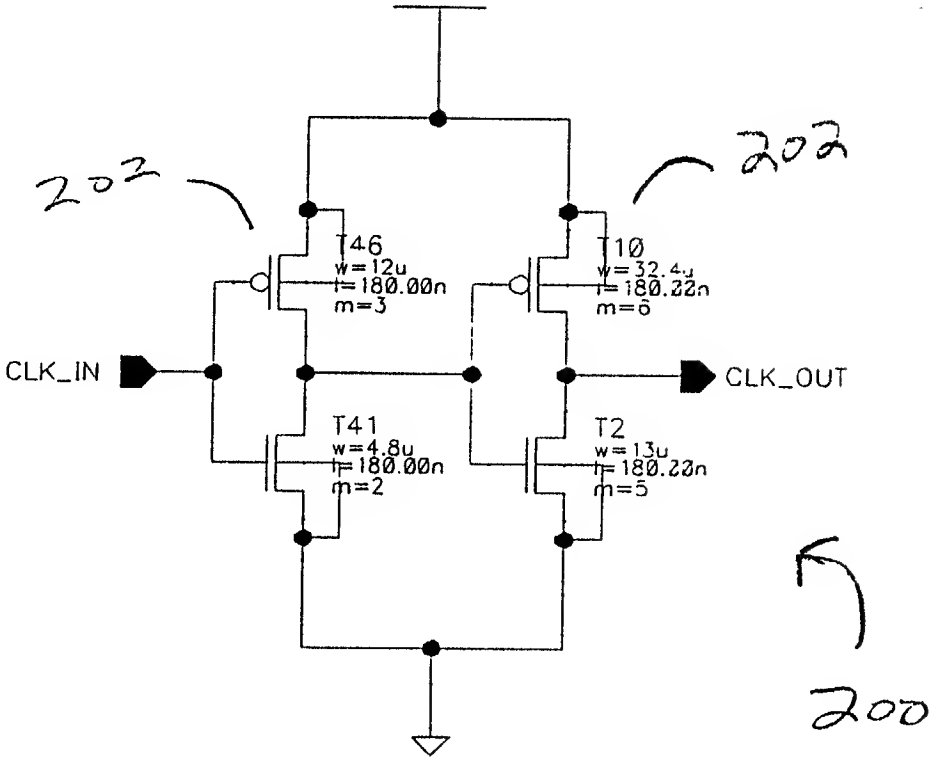


FIGURE 11

(FIGURE 31, page 71)

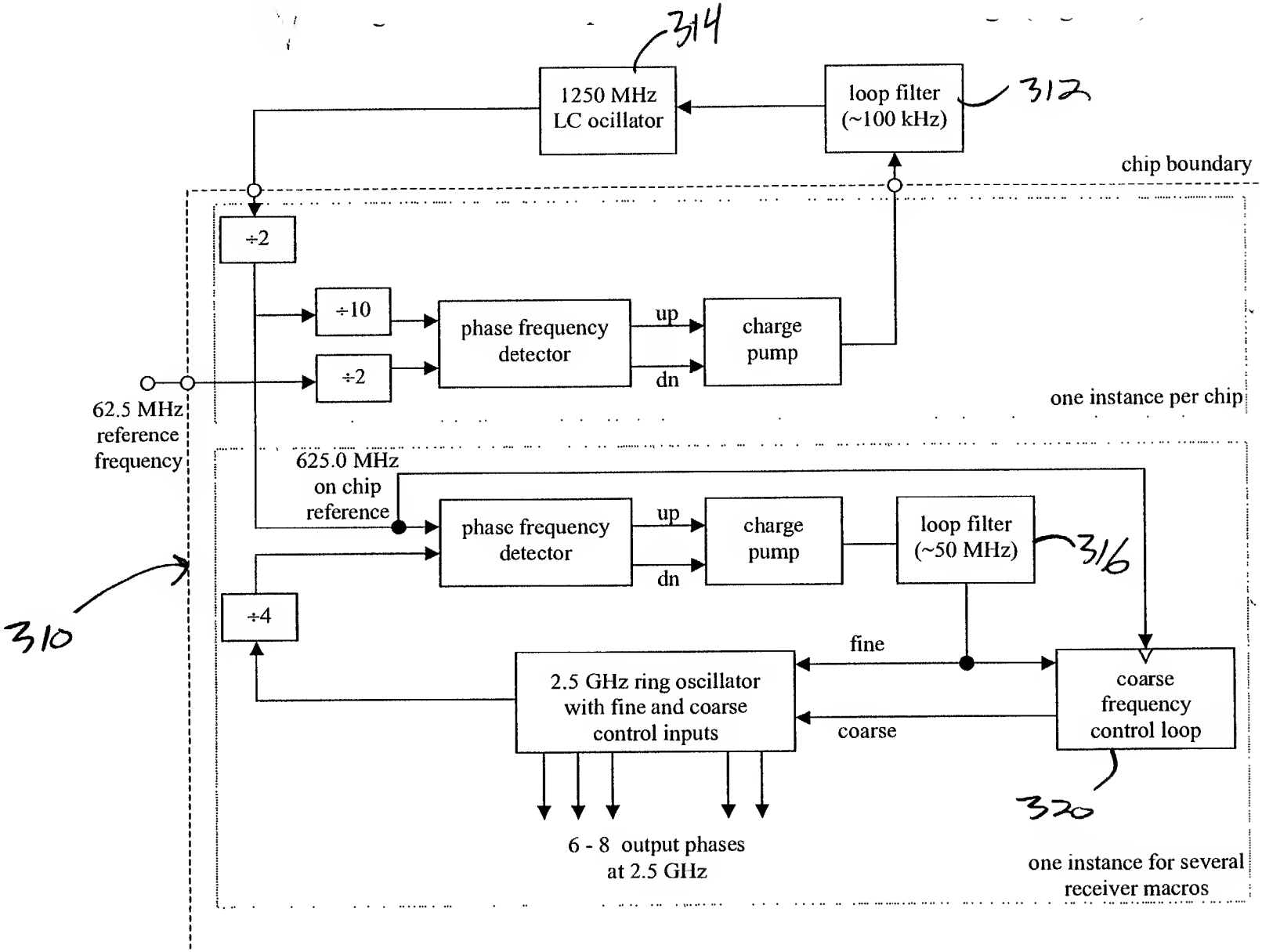


FIGURE 12

(FIGURE 7, SEINET SYS II)

12/26

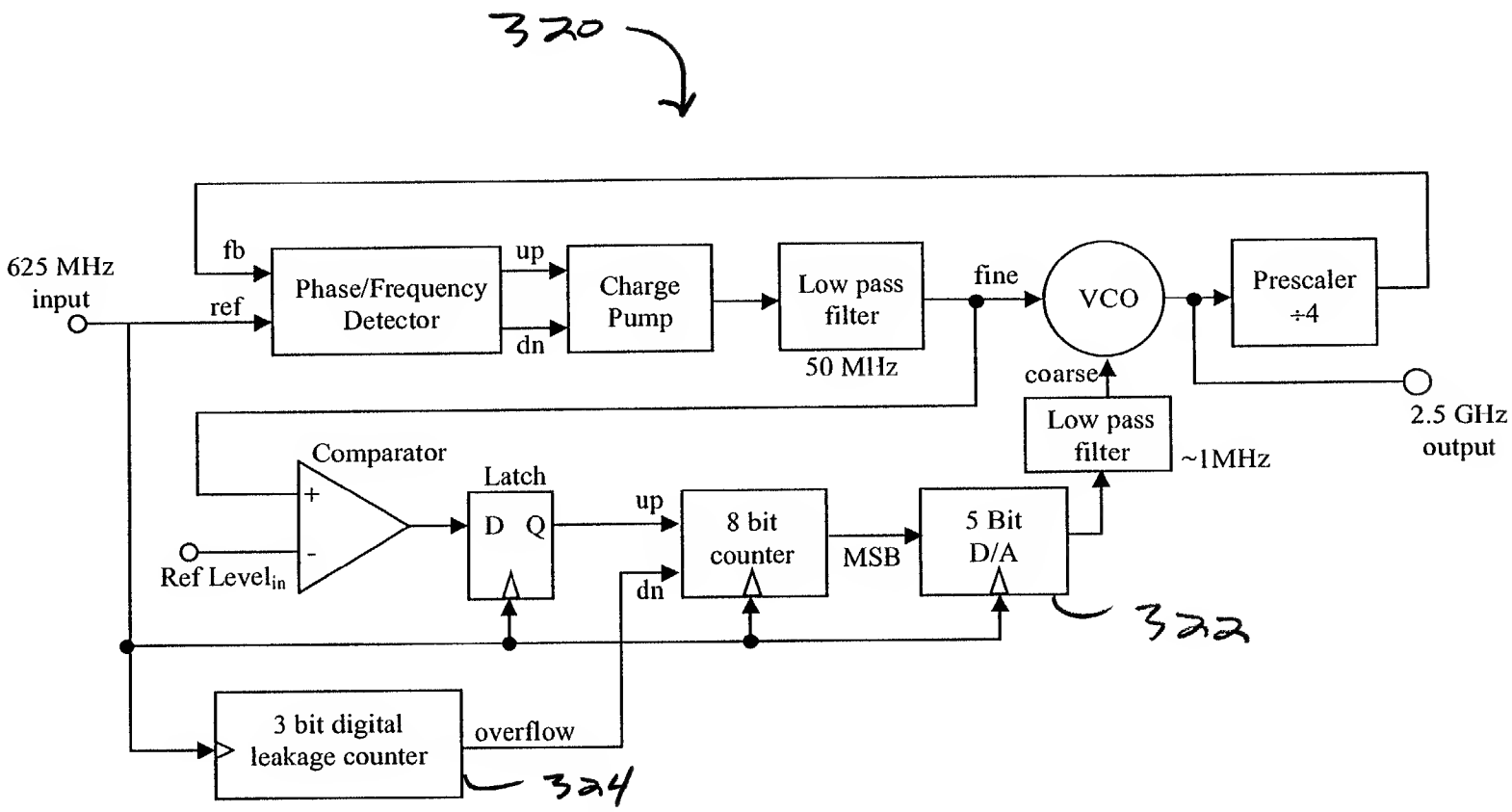


Figure 8: More detailed schematic of the dual loop PLL principle, JETNET SYS II

FIGURE 13

gure 32: RotatorTop, p76

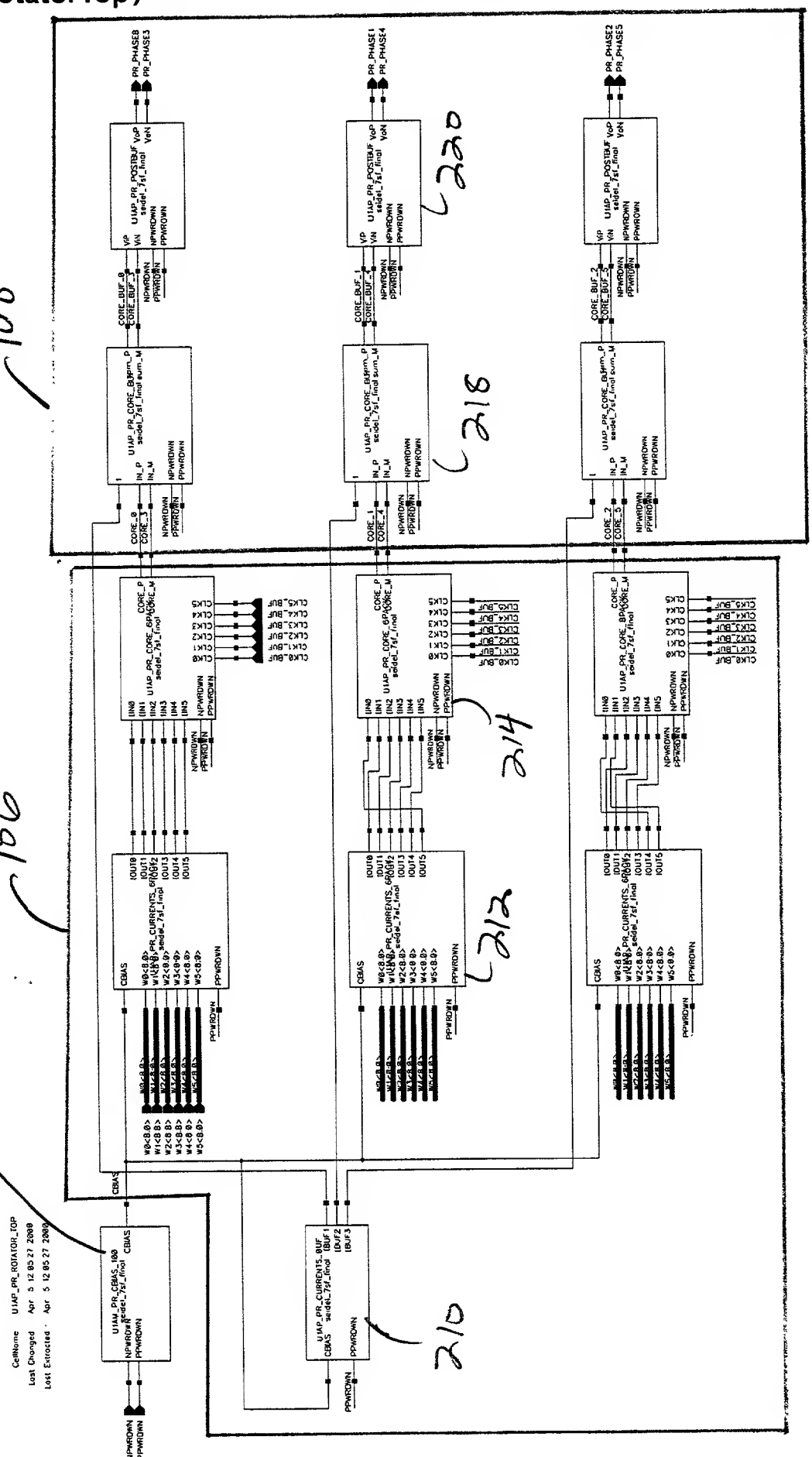
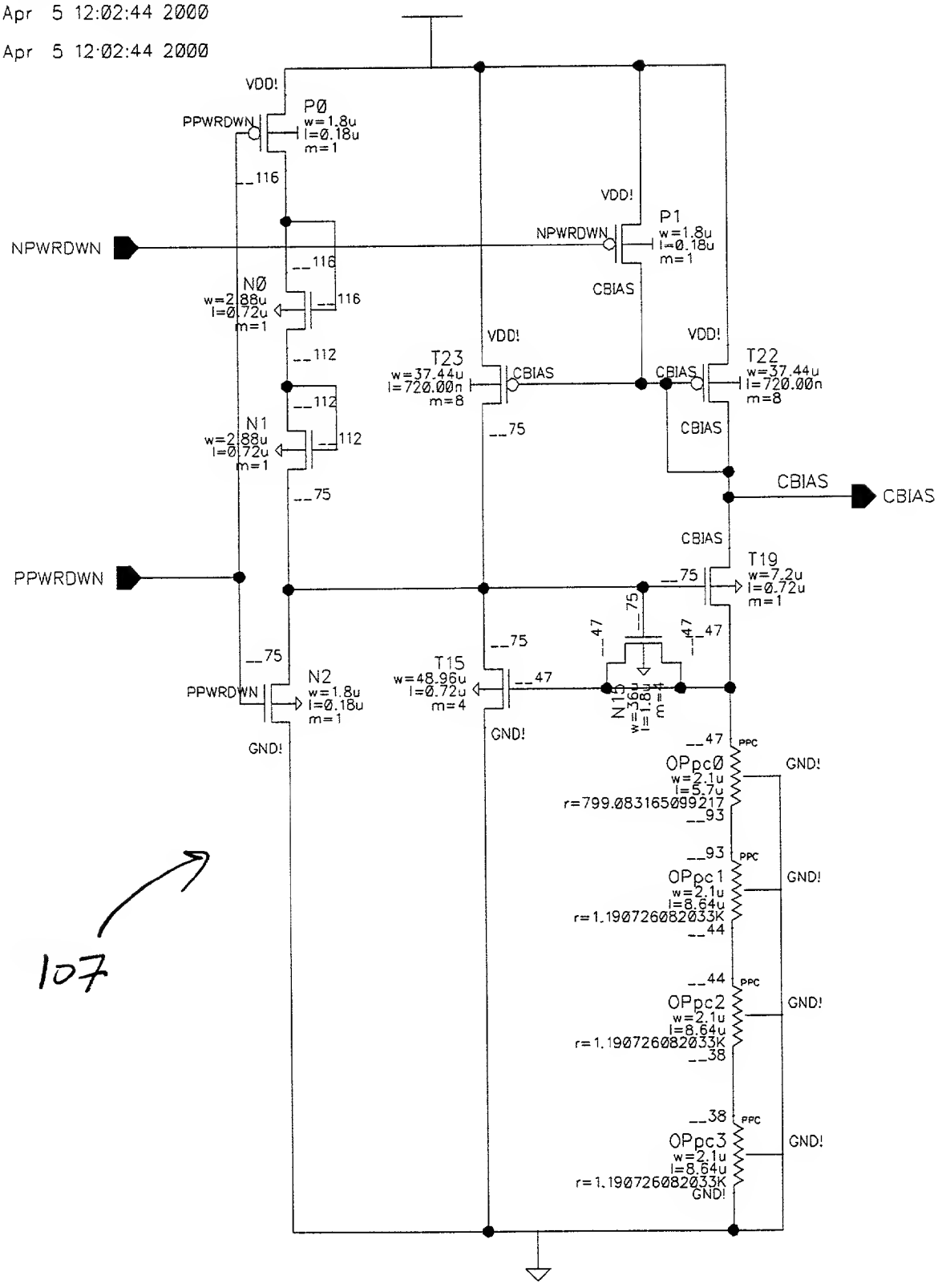


FIGURE 14

IName : U1AM_PR_CBIAS_100
hanged : Apr 5 12:02:44 2000
tracted : Apr 5 12:02:44 2000



107

FIGURE 15

CellName : OTAP_PR_CURRENTS_BUF

Last Changed : Apr 5 12:03:06 2000

Last Extracted : Apr 5 12:03:06 2000

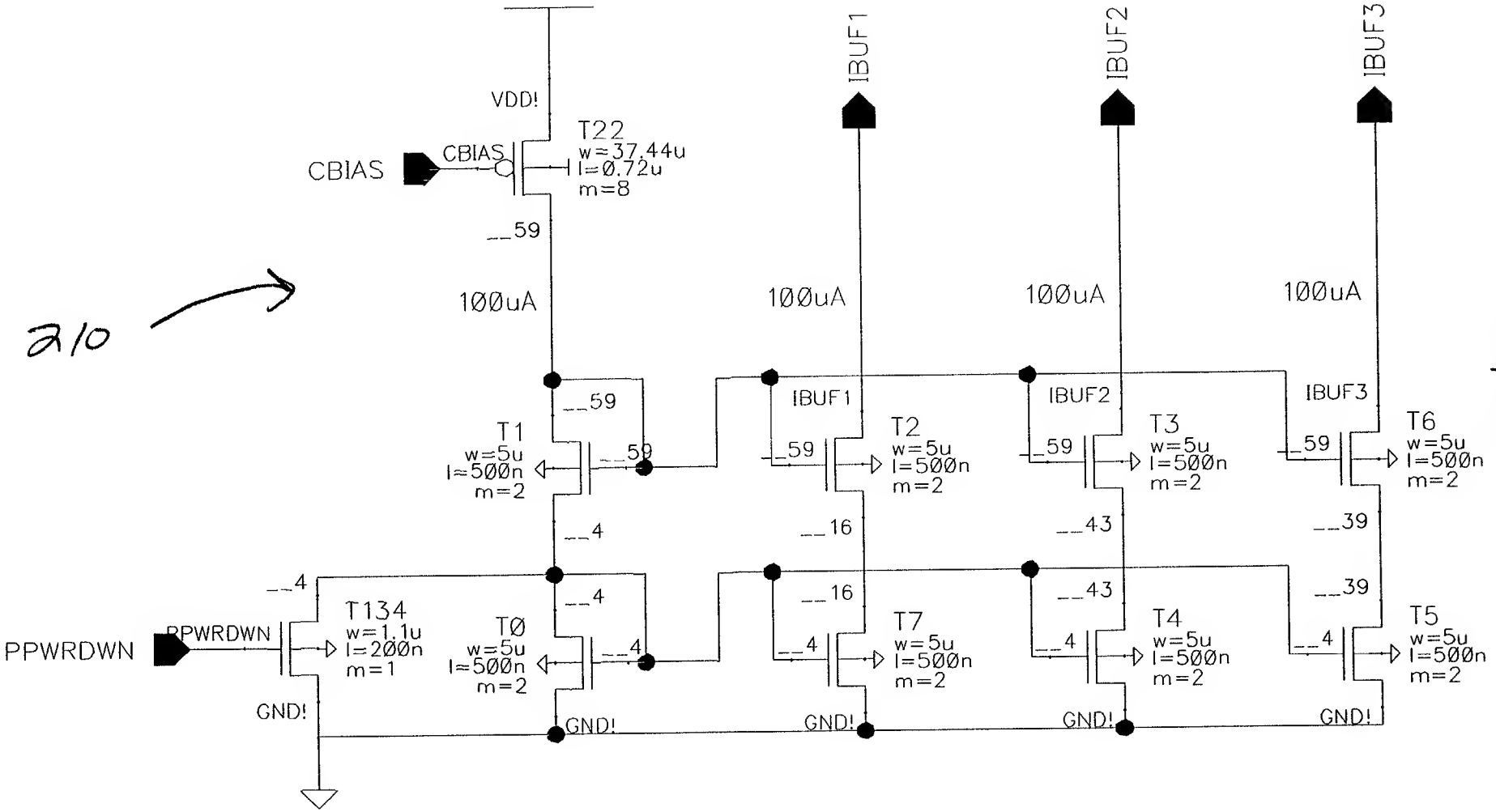


FIGURE 16

16/26

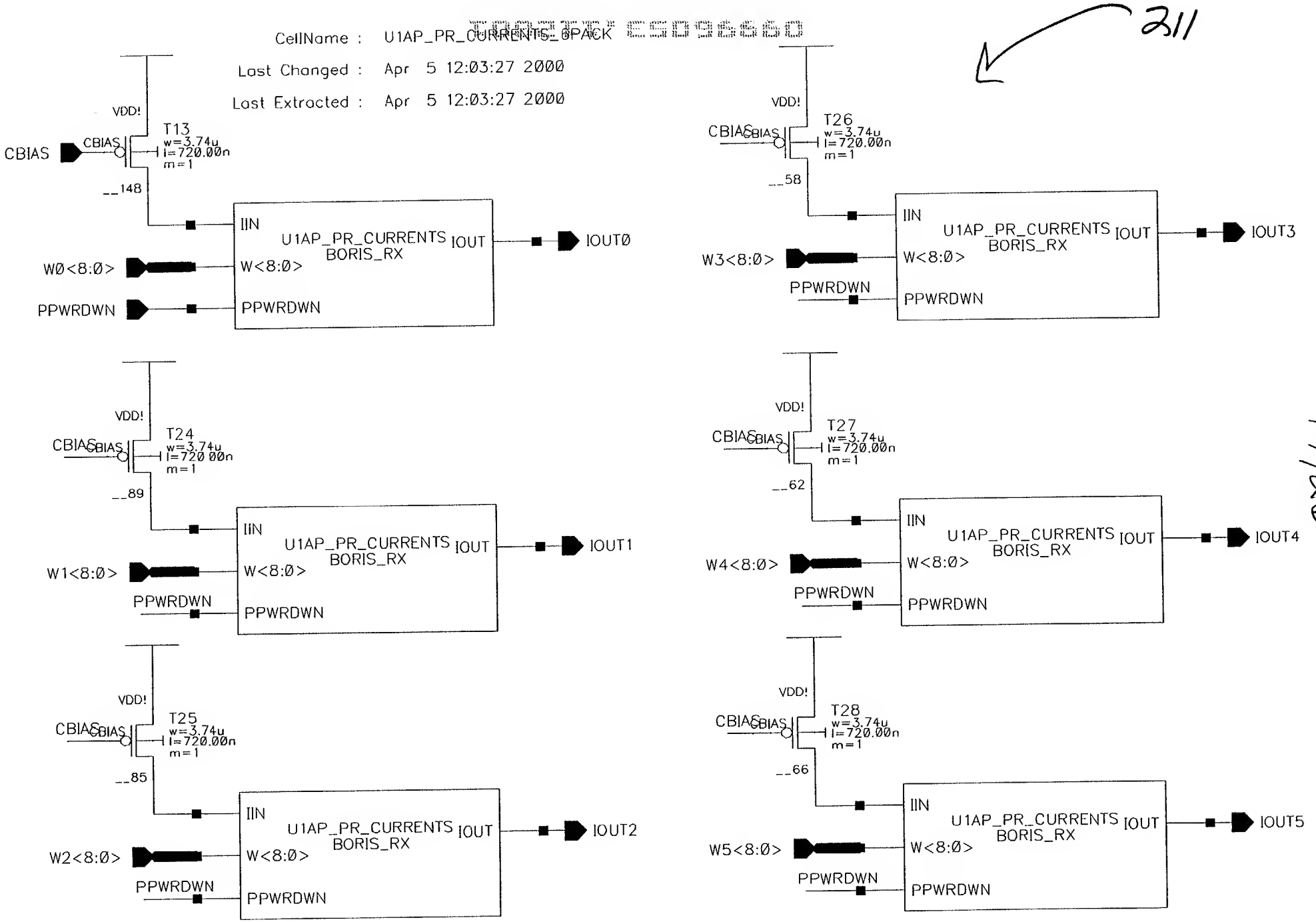

CellName : U1AP_PR_CURRENTS_8PACK
Last Changed : Apr 5 12:03:27 2000
Last Extracted : Apr 5 12:03:27 2000
211
VDD!
CBIAS
T13
w=3.74u
l=720.00n
m=1
__148
IIN
U1AP_PR_CURRENTS
BORIS_RX
IOUT
IOUT0
W0<8:0>
W<8:0>
PPWRDWN
T26
__58
IOUT3
W3<8:0>
T24
__89
IOUT1
W1<8:0>
T27
__62
IOUT4
W4<8:0>
T25
__85
IOUT2
W2<8:0>
T28
__66
IOUT5
W5<8:0>

FIGURE 17

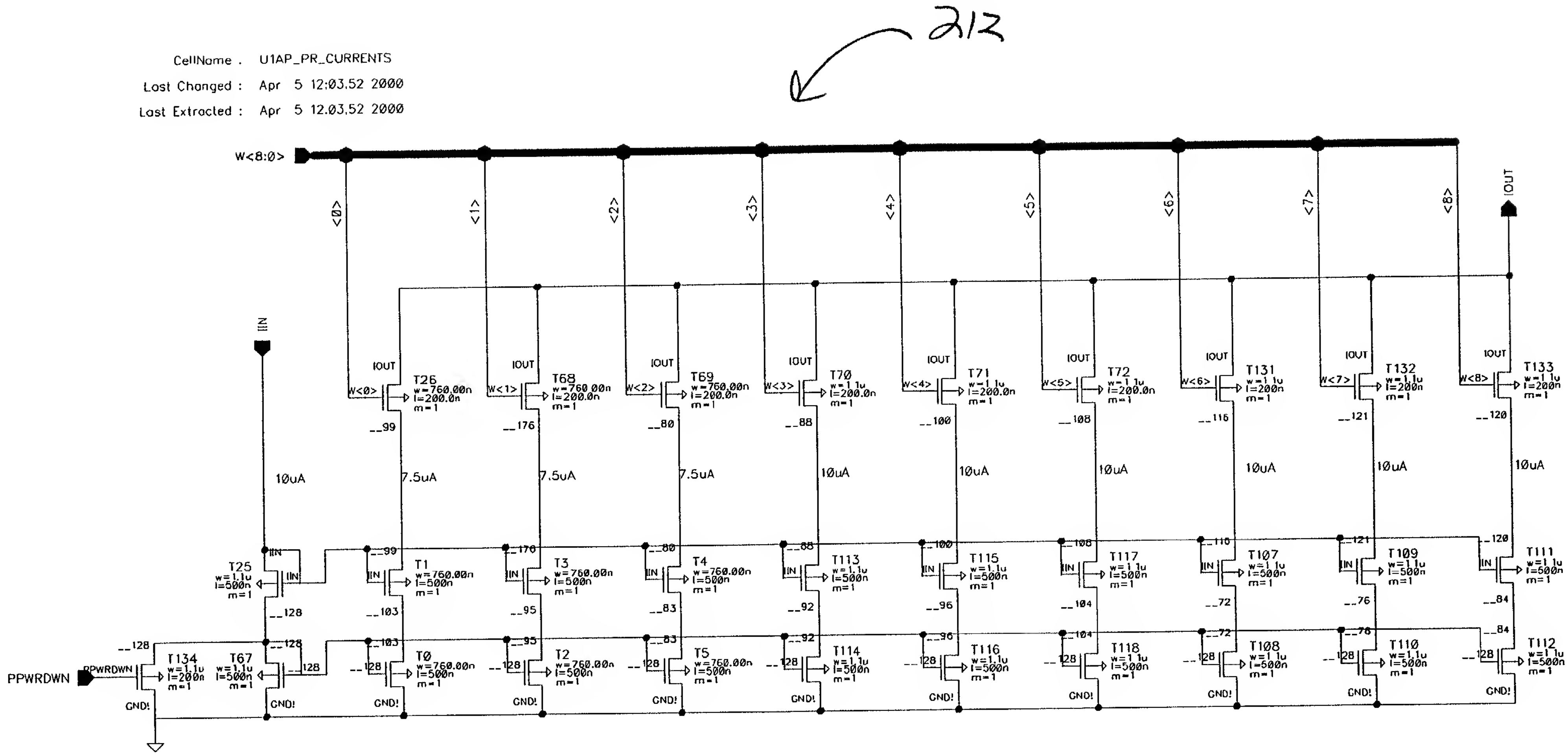

212
CellName . U1AP_PR_CURRENTS
Last Changed : Apr 5 12:03.52 2000
Last Extracted : Apr 5 12.03.52 2000
W<8:0>
IIN
IOUT
PPWRDWN
10uA
7.5uA
T25
T67
T134
T26
T68
T69
T70
T71
T72
T131
T132
T133
T1
T3
T4
T113
T115
T117
T107
T109
T111
T0
T2
T5
T114
T116
T118
T108
T110
T112
GND!

FIGURE 18

igure 37: Core 6Pack

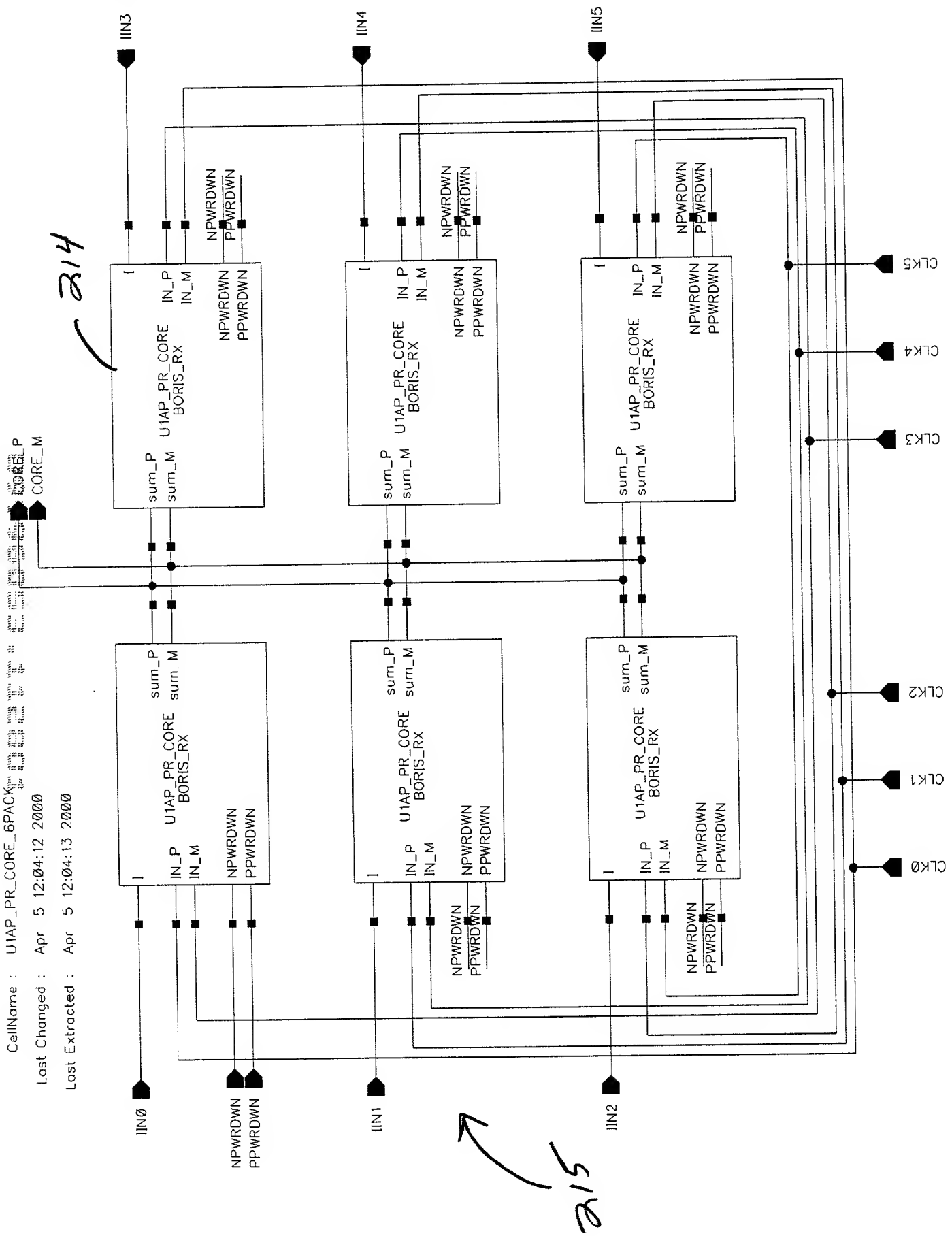


FIGURE 19

Figure 38: Core

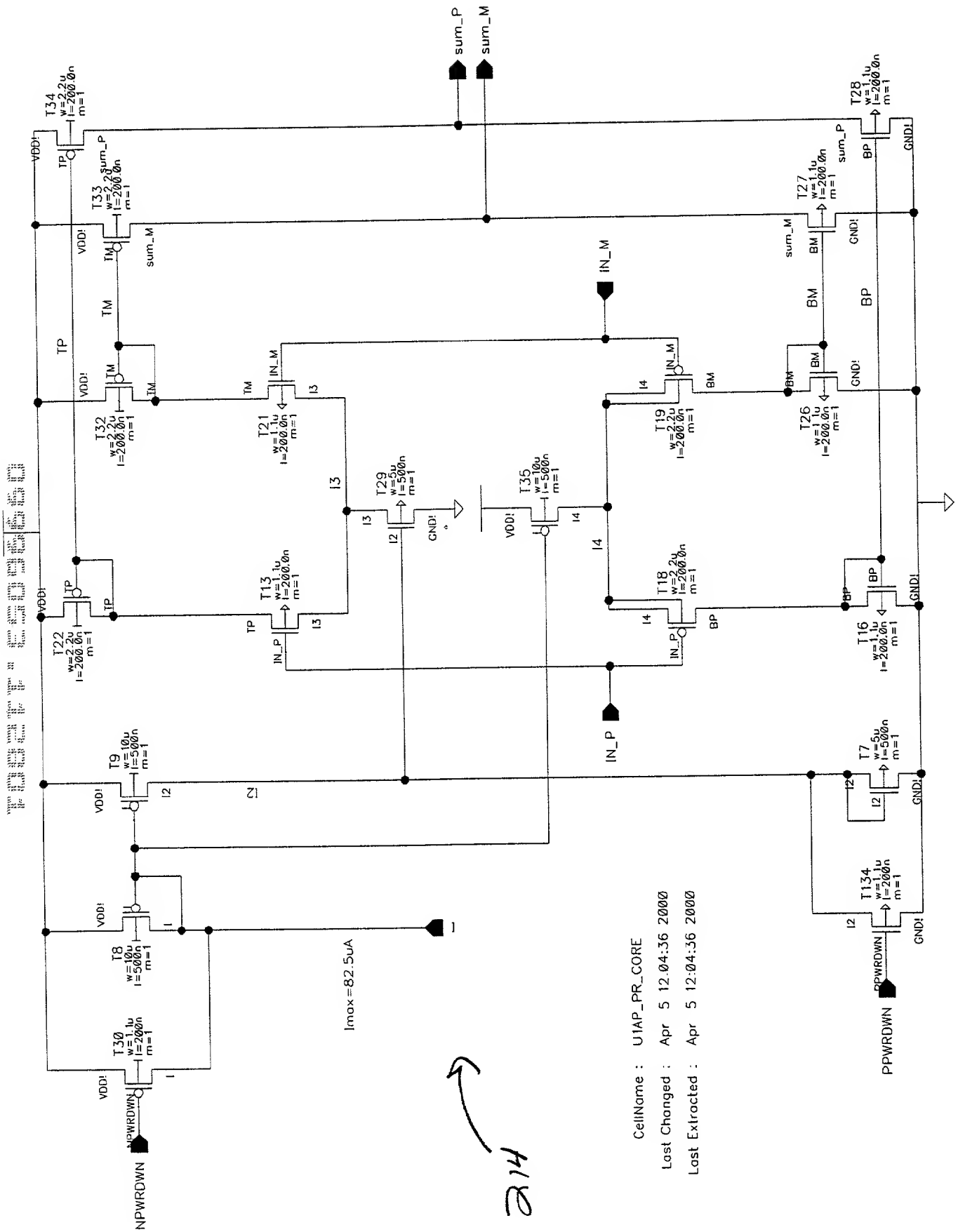


FIGURE 20

Figure 39: Core Buf

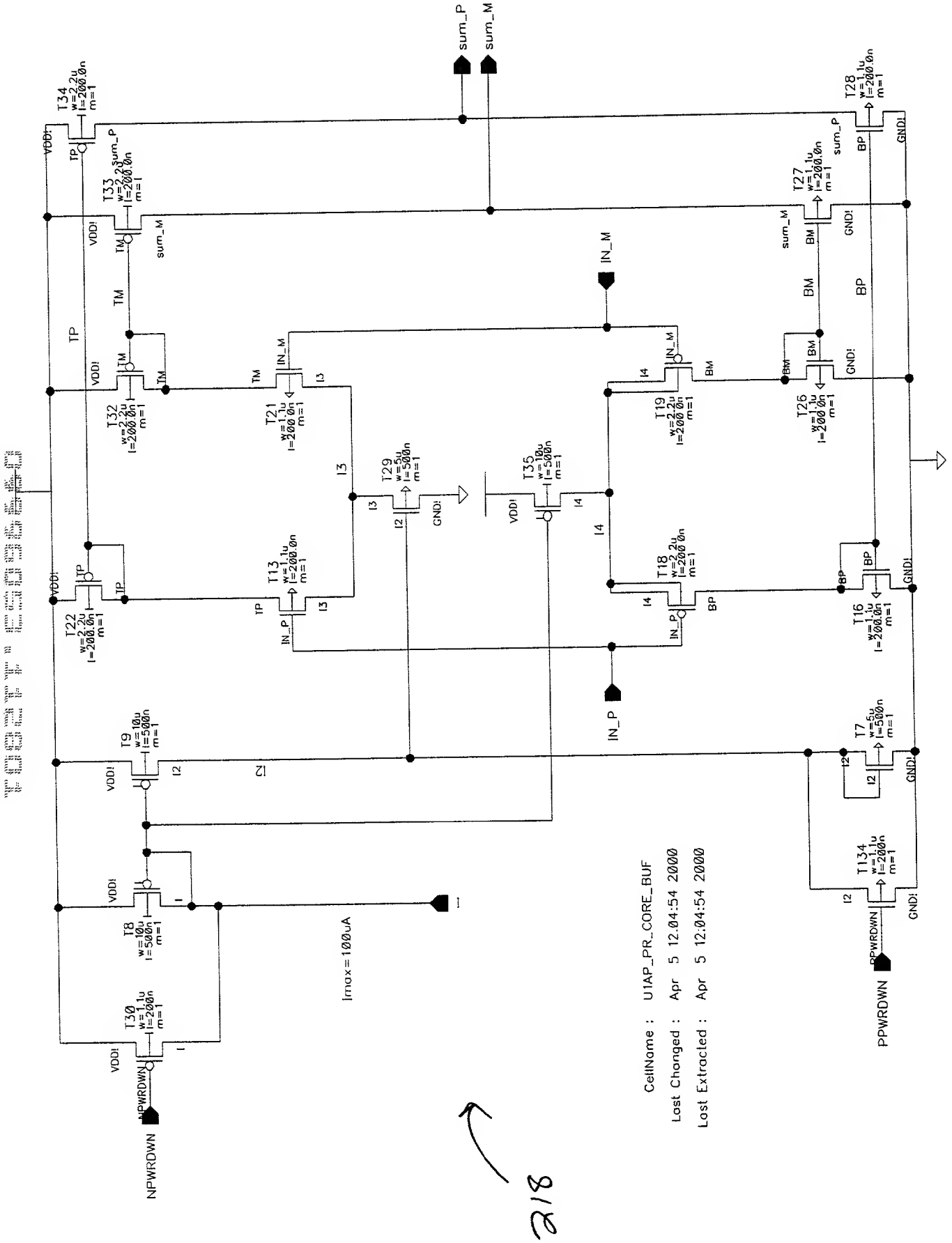


FIGURE 31

CellName : [illegible] f082ff" e5096660

Last Changed : Apr 5 12:05:18 2000

Last Extracted : Apr 5 12:05:18 2000

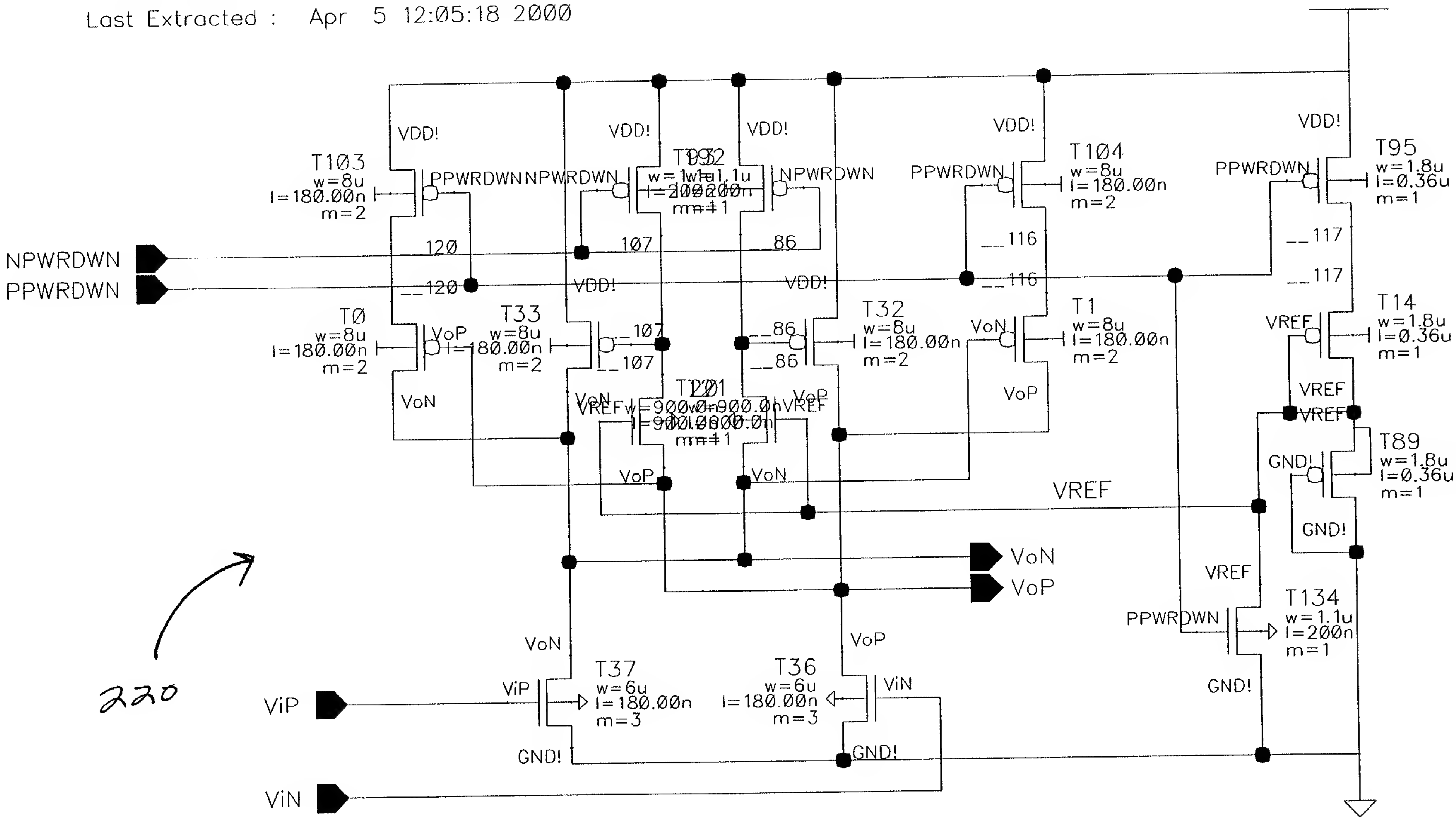


FIGURE 22

(FIG 40, p.84)

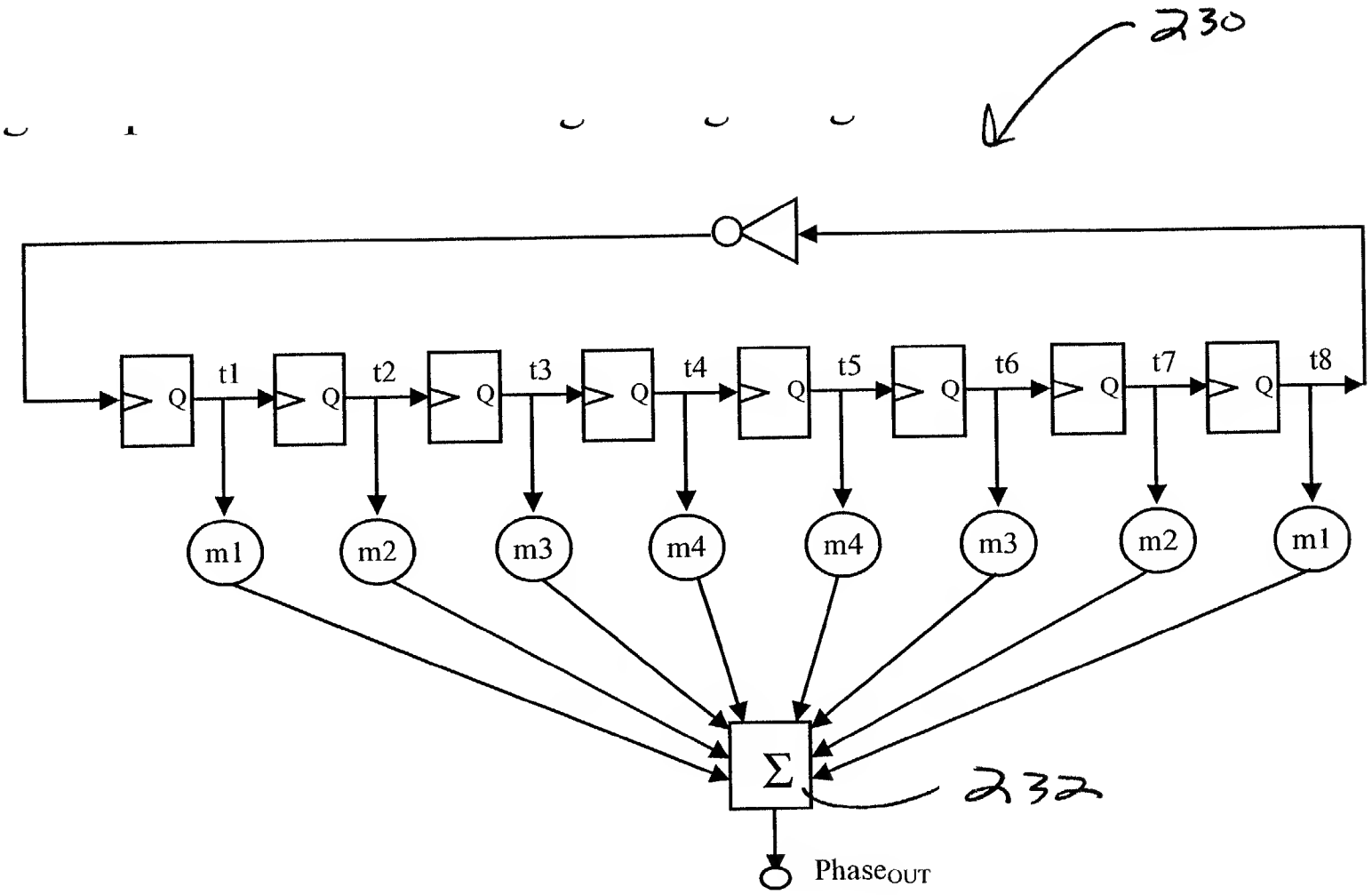


Figure 1: Eight stage ring oscillator with attached FIR filter

FIGURE 23

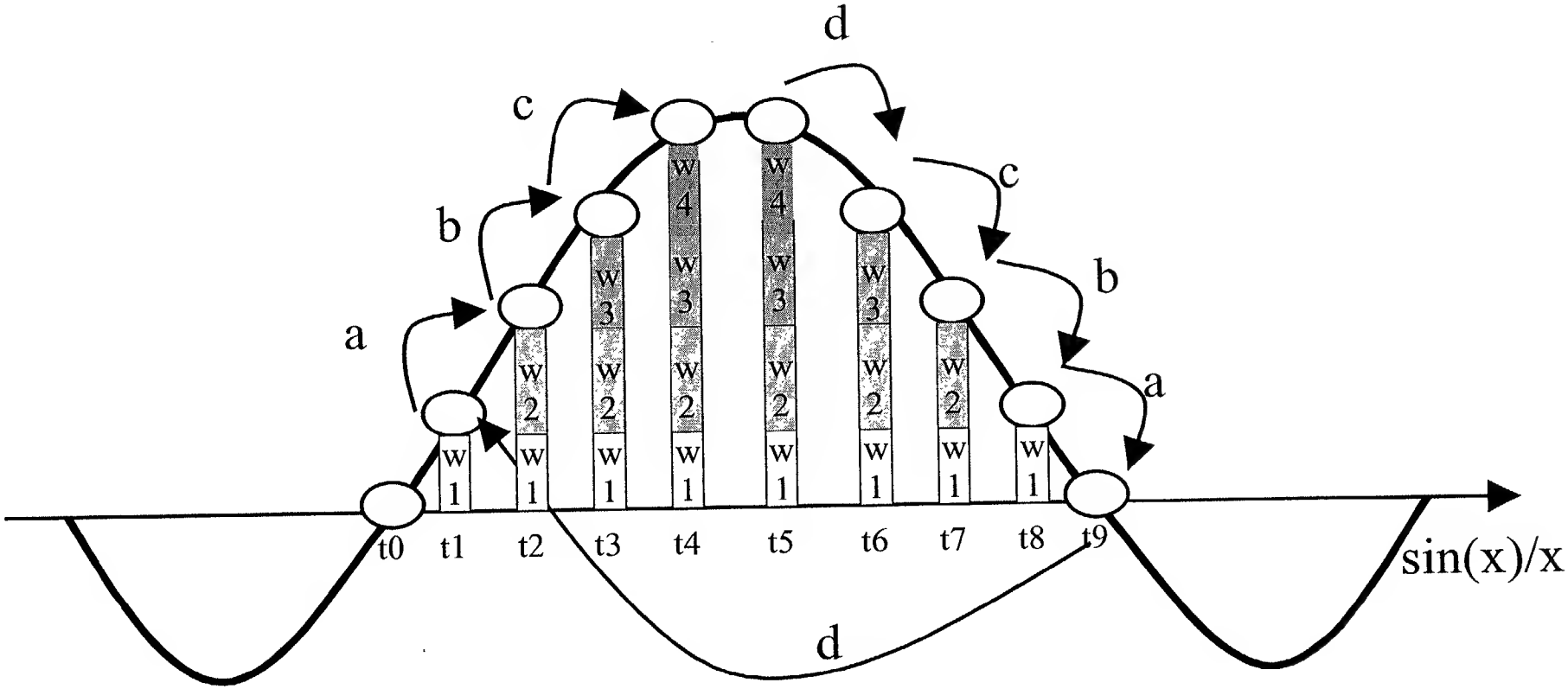


Figure 2: Rotation by one phase slice in four steps (a) to (d)

FIGURE 2A

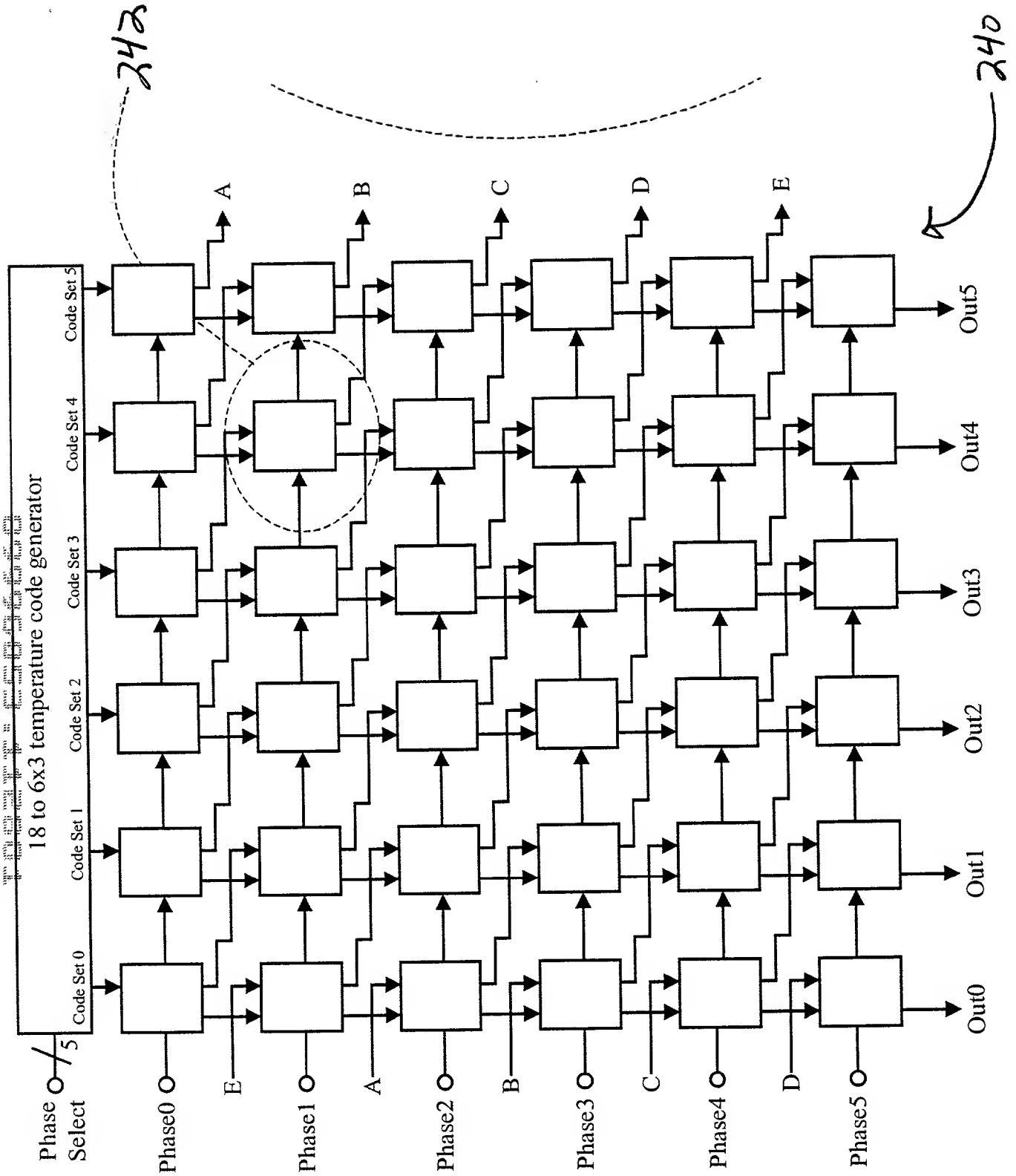

242
240
18 to 6x3 temperature code generator
Phase Select
5
Code Set 0
Code Set 1
Code Set 2
Code Set 3
Code Set 4
Code Set 5
Phase0
Phase1
Phase2
Phase3
Phase4
Phase5
A
B
C
D
E
Out0
Out1
Out2
Out3
Out4
Out5

FIGURE 35

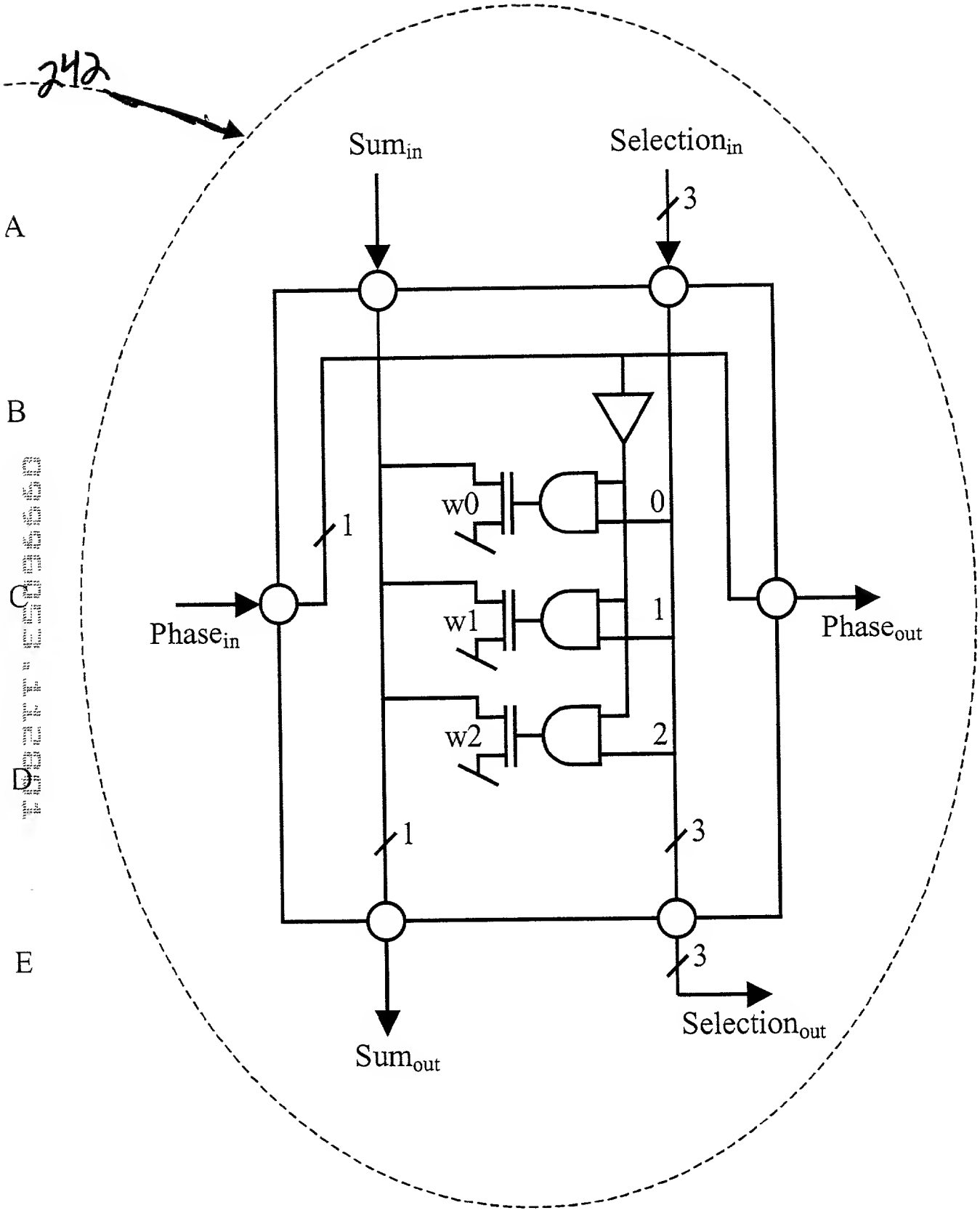

242
A
B
C
D
E
Sum_in
Selection_in
3
w0
0
1
w1
1
w2
2
Phase_in
Phase_out
1
1
3
3
Sum_out
Selection_out

FIGURE 26